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CDSP: AN APPLICATION-SPECIFIC DIGITAL SIGNAL PROCESSOR FOR THIRD GENERATION WIRELESS COMMUNICATIONS

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ABSTRACT

This paper presents an application-specific digital signal processor for third generation wireless communications. The processor architecture and instruction set are specially designed for the WCDMA system. These features make the proposed DSP outperform prior arts in terms of several crucial operations of wireless applications.

INTRODUCTION

Wireless communications related products are more and more popular in these years. In wireless devices, the programmable digital signal processors (DSPs) are widely used to support necessary system flexibility and upgradability. Several programmable DSPs have been presented for wireless communications [1-4]. These DSPs possess moderate processing capabilities for present second generation wireless systems, such as GSM or IS-95. However, the upcoming third generation WCDMA system intends to support real-time multimedia services, and thus demanding for much higher processor performance. The presented application-specific DSP, which is called CDSP, is a more powerful DSP with special instructions and processor architecture for third generation wireless communications. These key features make the CDSP consume much lower processor MIPS and therefore outperform prior arts [1-4] in terms of several crucial operations of wireless applications.

PROCESSOR ARCHITECTURE

Before designing the DSP architecture, the simulation of WCDMA system is firstly considered. After the simulation, several key operations that can be well executed by the DSP are then extracted. The CDSP is specially designed for symbol-rate I/Q channel data processing, and the block diagram of it is shown in Fig.1. Detailed design issues are discussed in the following subsections.

A. Memory Architecture and Pipeline Stages

Modified Harvard architecture including one program memory and two two-port data memories is used in CDSP. In single clock cycle, one instruction fetch from program memory, two operand reads from two two-port data memories, and two data writes back to two data memories can be performed simultaneously. There are five pipeline stages in CDSP: instruction fetch, instruction decode, operand read, execution, and write back.

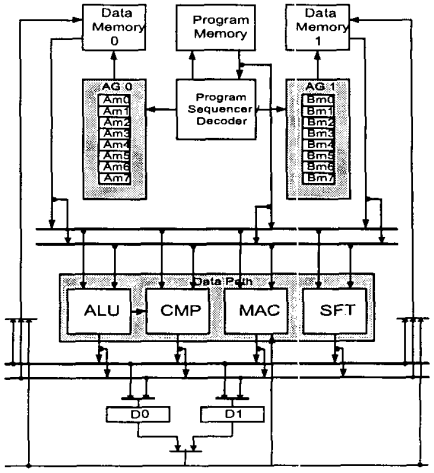

Fig.1 Block diagram of CDSP

B. Data Path with Sub-Word Parallel (SWP)

CDSP has four separate data path units: ALU (Arithmetic Logic Unit), MAC (Multiply Accumulate), CMP (Comparator), and SFT (Barrel Shifter). The inputs for ALU, SFT, CMP, and accumulator of MAC are 40-bit wide, and inputs for multipliers of MAC are 16-bit wide. The outputs of data path units can be stored into one of the two 40-bit accumulators (D0 or D1) or two data memories. All the executions of the four data path units are completed in single cycle. According to our simulation of WCDMA system, 6-bit word length is enough for symbol-rate data. Therefore, a normal 16-bit DSP data path can be divided further into two 8-bit data for I channel and Q channel respectively. By this SWP architecture of data path, the symbol rate I/Q channel data processing can be efficiently accelerated. Fig.2 shows the SWP architecture of the MAC.

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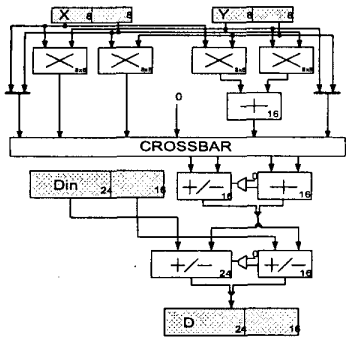

Fig.2 SWP architecture of the MAC unit

SPECIAL INSTRUCTIONS

Based on the WCDMA simulation results, several special instructions are designed for the key operations.

A. Channel Estimation for RAKE combining

In this operation, complex arithmetic such as multiplication and multiplication-accumulation are needed. In a normal 16-bit DSP, it will take six clock cycles to complete a complex multiplication that contains four multiplication operations and two addition operations. Since the CDSP supports SWP architecture, the four 8-bit multipliers of the MAC make it perform a complex MUL/MAC in one instruction cycle.

B. Viterbi Algorithm

Convolutional encoded data is decoded using the Viterbi algorithm on trellis diagram. There are two steps in Viterbi decoding process. The first step is the metric update, and the operation ACS (Add-Compare-Select) is used. This step is most time-consuming in Viterbi decoding. Both SIMD and SWP architecture are used to accelerate the ACS operation. The MAC bypassing the multipliers and behaves as a 24-bit and a 16-bit adder. The ALU also behaves as a 24-bit and a 16-bit adder. At the same time, the CMP selects and saves the minimum distance of previous calculated path distances to data memories. Therefore, two ACS operations can be completed in one clock cycle.

C. FIR Filtering

The SWP architecture of MAC also speeds up the FIR filtering operation by a factor of two. When performing FIR filtering, left two 8-bit multipliers, the middle stage 32-bit adder, and the accumulative 40-bit adder of MAC are active to complete the operation.

PERFORMANCE COMPARISON

Table 1 shows the performance comparison summary of CDSP with prior arts in terms of the convolutional decoding (R=1/2) for GSM, IS-95, WCDMA (3G), and also FIR filtering operation and complex arithmetic.

Table 1 Performance comparison summary

	TI C54x [1] (1 MAC)	TI C55x [4] (2 MACs)	LODE [2] (2 MACs)	MDSP-II [3] (2 MACs)	**CDSP (1 MAC)**
GSM Conv. (K=5)	0.58 MIPS	0.276 MIPS	0.44 MIPS	0.8 MIPS	**0.093 MIPS**
IS-95 Conv. (K=9)	6.57 MIPS	3.13 MIPS	5.2 MIPS	9.01 MIPS	**1.38 MIPS**
3G Conv. @ 384 kbps	263 MIPS	121 MIPS	208 MIPS	360 MIPS	**55 MIPS**
FIR (N-tap)	N Cycles	N/2 Cycles	N/2 Cycles	N/2 Cycles	**N/2 Cycles**
Complex MUL/MAC	4 Cycles	2 Cycles	2 Cycles	2 Cycles	**1 Cycle**

CHIP IMPLEMENTATION

A prototyping chip was implemented using cell-based design approach under TSMC 0.35um CMOS technology. The detail chip specification is shown in Table 2, and Fig.3 shows the die microphotograph.

Table 2 Chip specification

Technology	TSMC 0.35um CMOS 1P4M
Power Supply	3.3V
Maximum Frequency	40MHz
Core Area	5.6 x 5.6 mm^2
Power Consumption	500mW (3.3V, 40MHz)
Transistor Count	480K (DSP Core)
Internal Memory	One 1K x 28-bit Program Memory Two 2K x 16-bit Data Memories

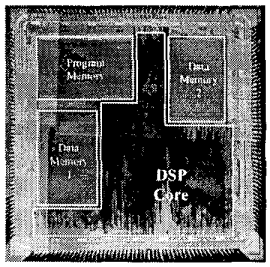

Fig.3 Die microphotograph

CONCLUSION

In this paper, an enhanced digital signal processor is presented for third generation wireless communications. The DSP outperforms prior arts in terms of several crucial operations of wireless applications.

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